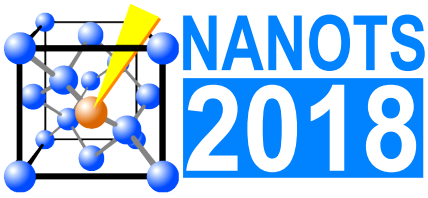
NANOTS2018— CALL FOR PAPERS (due: July 27)

The 38th Annual NANO Testing Symposium
19–20 November 2018
KFC Hall, Kokusai Fashion Center, Sumida-Ku, Tokyo, Japan
http://www-nanots.ist.osaka-u.ac.jp/



The institute of NANO testing invites nano testing professionals at all levels of experience from around the world to submit abstracts to NANOTS2018. NANOTS continues to be one of the leading technical symposiums for discussing solutions that improve the testing process of nano-scale devices and materials. For test designers, device manufacturers, and materials suppliers and testing equipment, NANOTS provides opportunities for testing professionals to network and learn the latest in the practical application of advanced nano testing strategies and methodologies to achieving nano-scale device dependability excellence. The two-day event of the 38th NANOTS (NANOTS2018) will consist of a symposium with a special invited talk, a special session, technical sessions, a commercial session, an equipment exhibition and an evening session. Papers for a special session and technical sessions are peer-reviewed and are selected based on a clear outline of problem, analysis, solution/results and conclusion. Presentations on original, non-commercial and non-published works are being solicited in the following technical scope.

Symposium Background

The NANO testing symposium is now in its 38th year since engineers and scientists facing the testing challenges posed by the then-advanced integrated circuit devices organized a symposium on Stroboscopic SEM and its Application in 1981. The name of symposium was changed to Electron Beam Testing Symposium in 1982, the LSI Testing Symposium in 1994, and the NANO Testing Symposium in 2013 as semiconductor technology and testing issues became more complex, challenging and global. The symposium is recognized as the foremost meeting dedicated to the testing of nano-scale devices covering the complete cycle from test design, manufacturing process, test, fault diagnosis, and failure analysis and back to process and design improvement. The symposium brings together engineers and scientists from industries and universities from all over the world to discuss recent progress and future trends.

Over the years, the symposium has evolved into the "annual meeting" of the testing industry. Technical sessions, complemented by tutorials, a commercial session and exhibits of test equipment and related services, have provided an opportunity for participants to see and discuss the latest available products and systems. Last year, 26 companies exhibited at NANOTS and 229 participants attended NANOTS. Now, more than ever, NANOTS is playing an increasingly important role as the industry's meeting place.

The NANO testing symposium is sponsored by the Institute of NANO Testing (http://www-NANOTS.ist.osaka-u.ac.jp/), in cooperation with the Institute of Electronics, Information and Communication Engineering, the Japan Society of Applied Physics, Reliability Engineering Association of Japan, and Union of Japanese Scientists and Engineers.

Technical Scope

Abstracts representing high quality original research are invited in the following areas.

ADVANCED DESIGN METHODOLOGIES FOR NANO TESTING

Design error diagnosis / Design for debug and diagnosis (DFD) / Design for manufacturing (DFM) / Design for reliability (DFR) / Design for testability (DFT) / Design for yield (DFY)

ADVANCED PROCESS TECHNIQUES FOR NANO TESTING

Interconnect: copper/low-k reliability / Wafer preparation / Physical characterization of wafers / Electrical characterization of wafers / Surface preparation: control and monitoring of surface treatment / Cleaning / Process control / Dopant diffusion / Oxidation and gate dielectrics: metrology of dielectric films / Optical lithography / Photomask fabrication: photomask qualification / Equipment reliability / In-line metrology: metrology for lithography processes, metrology for front end processes, interconnect process control, and in-FAB FIB / In-situ metrology / Yield modeling / Yield management / Electrical, Physical, and Chemical Characterization

ADVANCED NANO TESTING

System-on-chip testing / Memory testing / Delay testing / Low-power testing / Built-in self-testing / Software-based self-testing / Analog and mixed-signal testing / IDDQ testing / Burn-in testing / FPGA testing / High-speed I/O testing / RF testing

RELIABILITY PHYSICS AND ENGINEERING

Accelerated testing / Time-to-failure modeling / Time-to-failure statistics / Failure rate / Acceleration factor / Time-dependent dielectric breakdown

EFFECTS OF RADIATION ON INTEGRATED CIRCUITS

Radiation effects on semiconductor devices / Mitigation techniques

ADVANCED IC-LEVEL DEBUG AND DIAGNOSIS

Silicon debug / Defect diagnosis / Cause-effect analysis / Effect-cause analysis / Scan chain diagnosis / Logic BIST diagnosis / Memory diagnosis and built-in self-repair

ADVANCED CIRCUIT EDITING FOR DEBUG AND DIAGNOSIS

Focused Ion Beam / Layout-database-driven navigation system

ADVANCED PROBING TECHNOLOGIES FOR DEBUG AND DIAGNOSIS

Die exposure technique / Mechanical probing / Injection-based probing: e-beam probing, laser beam probing (laser voltage probing, resistance change (OBIRCH, SDL)) / Emission microscopy / Emission-based probing: infrared emission microscopy (IREM), picosecond imaging circuit analysis (PICA), time-resolved emissions (TRE) / Others

PHYSICAL ANALYSIS TOOL FOR FAILURE ANALYSIS

Package analysis / Deprocessing / Parallel polishing / Cross-section analysis / Microscopy / Transmission electron microscopy (TEM) / Others

CHEMICAL CHARACTERIZATION FOR FAILURE ANALYSIS

X-ray analysis (energy dispersive) / Auger / Secondary ion mass spectroscopy (SIMS) / Microspot Fourier transform infrared spectroscopy / Others

FAILURE MECHANISMS IN NEW MATERIALS AND TRANSISTORS

Process-related issues / Hot carriers / NBTI / PBTI / Passivation stability / Dielectric integrity / High-k gate oxides / Latchup / ESD / Metal migration: mechanical and thermal aspects / Low-k dielectrics and Cu interconnects / Reliability related to nanotechnology

ECONOMICS OF NANO TESTING

Economic effects / Economic models / The learning curve / Technological driving forces / Factory and equipment economics

TESTING FOR NEW DEVICES (including Devices for Biological Science, Medical Applications and Health Monitoring)

Micro Electro Mechanical Systems (MEMS, BioMEMS) / Sensors / Liquid Crystal Display (LCD) / Nano-tube / PRAM / RRAM / FRAM / Others

ADVANCED TESTING EQUIPMENT AND SYSTEMS

Transmission electron microscope (TEM) / Scanning electron microscope (SEM) / Focused ion beam (FIB) / Scanning Probe Microscope / Others

CASE STUDIES OF NANO TESTING

Electrical characterization / Die exposure / Package analysis / Global failure site isolation / Probe failure site isolation / Defect exposure / Physical inspection / Chemical analysis

Special sessions

— November 19, 2018 —

Special invited talk: "Ultra-low power data collection system (tentative)," by *Dr. Shozo Saito, Chairman, Device & System Platform Development Center Co., Ltd.*

Invited talk: "What value adding is expected for power devise?" by *Dr. Katsuaki Saito, Hitachi Power Semiconductor Device, Ltd.*

— November 20, 2018 —

Panel discussion: "Machine learning — Its possibilities and limitations (tentative)"

Invited talk: "A new international system device roadmap for cloud/IoT-edge solutions," by *Dr. Yoshihiro Hayashi, Chairperson of SDRJ (Renesas Electronics Corporation)*

Invited Talk: "Attosecond electron imaging," by *Dr. Yuya Morimoto, Ludwig-Maximilians-Universität München*

Instructions to authors for technical sessions

Abstracts are welcome from all those involved in all areas of nano testing. Original papers co-authored by a user and a supplier and/or academia that demonstrate innovative, practical solutions for advancing nano testing are highly encouraged. Authors must provide an extended abstract of no more than one page of text (A4 size paper, max. of 1000 words, MS Word or pdf) with an additional page including supporting data and figures. The abstract should provide an overview of: the problem; current practice in industry and its limitations; and proposed solution, as well as provide a brief summary of results. Include title, author(s), company affiliation(s), contact information, five key words and at least one AREA as listed on this call for papers. Abstracts are due July 27, 2018 and should be submitted on-line. Please note that abstracts and papers must be in English or in Japanese. For a sample abstract and further author instructions, please visit our website: http://www-NANOTS.ist.osaka-u.ac.jp/

All abstracts will be peer reviewed by the NANOTS committee according to the following criteria:

- Originality of work,
- Specific results achieved and described, and
- Potential impact and interest to attendees.

Notification of acceptance, including additional author instructions, will be sent via e-mail by September 14, 2018. A final, company-approved manuscript and copyright form must be sent electronically by October 19, 2018 in order to be published in the NANOTS2018 proceedings.

Instructions for equipment exhibition and commercial session

The Symposium will feature the latest in service providers, equipment manufacturers and suppliers. A large exhibit floor will give the opportunity to key-vendors to represent the core business area in these fields. Furthermore, a commercial session will give the opportunity to introduce new products with short presentation.

Applicant for equipment exhibition and a commercial session must be an associate member of the Institute of NANO testing. Applicants for a commercial session must provide an abstract of no more than one page of text (A4 size paper, max. of 1000 words, MS Word or pdf). The abstract should provide an overview of new product. Include title, author(s), company affiliation(s), contact information, several key words and at least one AREA as listed on this call for papers. Abstracts for a commercial session (short presentation) are due July 27, 2018 and should be submitted on-line. For further information concerning an associate member, the equipment exhibition and a commercial session, please visit our website: http://www-NANOTS.ist.osaka-u.ac.jp/

Evening Session

The evening session of NANOTS will provide international conference reports and so on. It will be held on the first-day night in the KFC Hall. Registration fee includes one ticket to evening session of NANOTS. For further information, please visit our website: http://www-NANOTS.ist.osaka-u.ac.jp/

Symposium Registration

We strongly encourage you to register on line by using our website: http://www-NANOTS.ist.osaka-u.ac.jp/. The online registration system will be open in the middle of September 2018.

NANOTS committee (steering & program)

Chair:

K. Nakamae – Osaka University

Members:

Y. Goto – Toyota Motor Corp.
Y. Higuchi – Hitachi, Ltd.
S. Iida – Toshiba Memory Corp.
T. Koyama – Renesas Semiconductor Manufacturing Co., Ltd.
S. Motegi – Thermo Fisher Scientific K.K.
K. Nikawa – Kanazawa Institute of Technology
Y. Ose – Hitachi High-Technologies Corp.
M. Suga – JEOL, Ltd.
H. Terada – Hamamatsu Photonics K.K.
Y. Yamazaki – NGR Inc.

Secretary

K. Miura – Osaka University
Y. Midoh – Osaka University

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